Design for Testability for SoC Based on IDDQ Scanning

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Abstract – One DFT solution for systems on chip, based on IDDQ measuring concept is presented in this paper. The application of Reconfigurable neural networks off chip enables also good diagnostics capabilities. The solution is to be implemented in few digital blocks of the tree phase power meter IC and realized using CMOS035 technology. The simulation results obtained using Cadence Virtuoso show good performances of the solution.

I. INTRODUCTION

IDDQ testing is an approach used in electronics to test CMOS integrated circuits. As opposite to all other testing techniques which measure voltage levels in the circuit, this one is based on measuring electrical current. Generally, CMOS circuits consume power only when their logic values are changing [1]. IDDQ testing is based on this fact. CMOS IC will drain a very low level of current in this quiescent state, typically in the fA range for small to the pA range for complex SoCs. Most manufacturing defects present in the circuit will likely cause the measured current to raises from these value by several orders of magnitude or more.

Any block or a subcircuit in an IC, must have power lines, which are usually accessible for observing and measurement. That is why IDDQ testing has the property of an automatic observability: Any abnormal behavior within a circuit does not need to be propagated to a device output for detection - it will be evident after the quiescent current measurement.

The technique is seen as a valuable supplement to other methods of circuit testing since it allows the detection of certain types of fault which might not be found using voltage-based techniques. Advantages of IDDQ testing are known for a long time. Test generation is much easier since the automatic observability is guarantied [2]. Power supply pins are always available for observing [3]. The only task of test generation is to activate the fault. IDDQ test can detect many other kinds of faults, which cannot be detected with a standard functional or structural test, based on a stuck-at fault model. IDDQ test is the only way to detect the following faults and defects: bridging faults, gate oxide defects, gate leakage within a transistor, shorts between any two of the four terminals of a MOS transistor, parameter defects – which does not affect the logic function of the circuit, but may have an effect to reliability, causing delay faults or stuck-open faults. Nevertheless, IDDQ testing has disadvantages that must be considered before this test is applied [4]. Firstly, since normal IDDQ is very low, it must be measured very precisely. Secondly, by the nature, the IDDQ test is aimed for static devices, while dynamic circuit, pull-up or pull-down resistors, speed optimized circuitry should be avoided. However the both drawbacks may be diminished, if IDDQ is incorporated in specific DFT technique.

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II. IDDQ TESTING PRINCIPLES

There are tree different IDDQ test applications [1]. The first considers doing IDDQ test during the usual circuit testing. It means that this value is measured after every test vector. This is very useful for the prototype testing. The second method is a selective IDDQ. IDDQ measurements are performed here on a selected subset of the entire test sequence. The third is a supplemental IDDQ where specific set of vectors is chosen to enable improved IDDQ defect observability. This is performed after the functional test.

As mentioned before, CMOS integrated circuits have no direct current flow from V_{DD} to GND in the quiescent state, or when there is no transistor switching. If a circuit has significantly high IDDQ, it is considered as a defective. A threshold is defined as a value which helps to differentiate defective circuits from the non-defective ones. Setting this value has a great importance in sense that an improper threshold value results in unrealistic number of either defective or good chips. This can further lead in lowering the yield and profit.

This paper suggests including IDDQ measurements into SoC prototype testing and verification. Therefore a good DFT strategy is necessary. One possible solution of this problem will be given next.

III. SCAN BASED IDDQ TEST SOLUTION

The block diagram of IDDQ scanning DFT solution is shown in figure 1.

The basic idea is to implement IDDQ scan chain for separate blocks (*block under test*, BUT in Fig. 1) of SoC. As shown in the figure, the test/measurement circuitry consists of tree blocks. BICS (built-in current sensor), AMUX (analog multiplexer) and test control circuit. Each BUT is connected to a small BICS block via its power line. BICS should not have influence to the functioning of the BUT, either during the test or normal operating mode.

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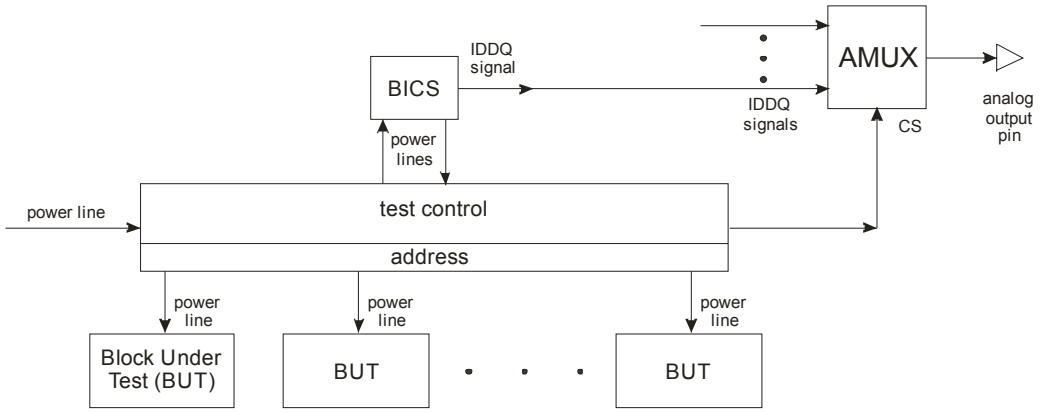


Fig. 1. DFT that enables IDDQ scanning.

Figure 2 shows the general structure of the BICS cell. It consists of four blocks: current sensing device, switching circuit, current-to-voltage converter and an amplifier. A current sensing device (for example current mirror based circuit) measures the current, whenever its chip select signal is activated. The current is then converted into voltage equivalent. This value is then sent to an analog multiplexer that can forward the signal to the output pin of the IC.

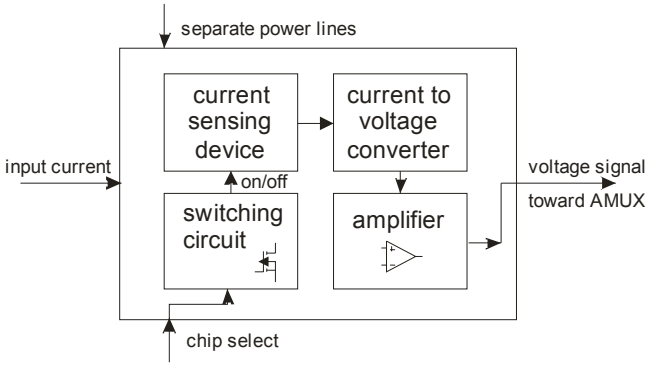


Fig. 2. BICS internal structure.

Afterward the voltage can be acquired and processed in a diagnostics unit, placed outside of the IC. The test control unit (TCU) controls all these activities. TCU addresses BUT to be tested, and one by one, controls the scanning of their IDDQ. It selects the particular BUT, activates its BICS cell, simultaneously activates the corresponding AMUX and exports the scanned value to the IC output.

In order to reduce area enlargement due to the test circuitry, one BICS cell share several adjacent BUT blocks. Test control circuitry forces the power line signal of the chosen BUT to go through the common BICS. Outputs of several testing structures are gathered through an analog multiplexer to pass IDDQ information to only one output pin.

As mentioned above, only one BICS measures the current of few BUTs. Figure 3 presents part of the circuitry that controls switching from one of the BUTs to BICS. In normal operating mode, analog multiplexer and demultiplexer leads the power line directly to the BUT bypassing the BICS. When particular BUT is to be tested, its power line is directed through BICS and enables observing its IDDQ.

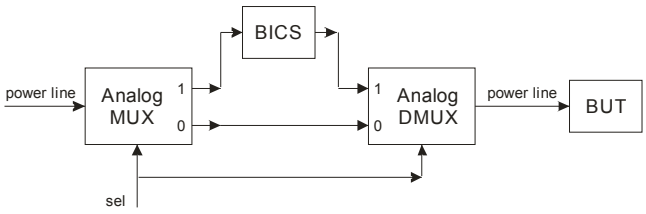


Fig. 3. Part of the Test Control Unit.

According to the extremely restrictive primary requirements, the BICS cell is the most complex DFT component to design. Firstly, the sensor should affect BUT function as less as possible. Namely, the sensor should maintain the correct power supply voltage to the block power lines, during the normal functioning as well as during testing. The voltage swing of digital signal is reduced due to the voltage drops on Vdd and Gnd. Secondly, as Iddq is small, the sensor must be precise enough. Thirdly, in order to avoid any additional interference between BUT and BICS cell, their power lines should also be separated. And finally, the frequency range of the BICS should be wide enough to ensure good detection of the potential current picks during transitions

There are few available realizations of this block. Primary BICS blocks were based on the current mirroring principle. One such solution based on NPN bipolar transistors is given in [5]. The problem with this circuit is that NPN bipolar transistors are very difficult to create in a standard CMOS process. They also provide a narrow frequency range, which bounds the measurements. A better solution is given in [6]. This solution is based on the use of a CCII+ arrangement and has much higher accuracy and a wider operating range. Further improvements of the BICS are given in [4], [7], and [8].

Aside from detection of digital blocks malfunction within the SoC, the proposed DFT technique offers good diagnostics capability, as well. Namely, the suggested technique can be easily extended to a DFD (design for diagnostics) system by adding the acquisition and diagnostics block outside the SoC. An interesting and effective diagnostics solution utilizes reconfigurable neural networks. Explicitly, an artificial neural network can be trained to recognize faulty behavior of the circuit and to detect where and why the problem occurred. The network can relay on software or hardware implementation enhanced with a dictionary of defects. Detailed explanations of such diagnostic units are given in [9], [10] and [11]. The application of the reconfigurable neural networks ensures that one neural network is used for diagnostics of several blocks since its weight coefficients can easily be switched, according to the address of the block to be tested.

The DFT solution for IDDQ testing is very similar to the Boundary Scan concept by its structure [12]. It has a BISC cell instead of Boundary Scan cell. And the test logic controls the testing of the digital SoC components [13]. These two solutions can be easily merged into a unique testing environment, as well. The IDDQ testing starts by applying the input test vectors into the boundary scan cells connected to the inputs of the digital logic. Simultaneously the BICS measures the current through power lines and passes the results to the diagnostic unit when the logics reaches the quiescent state.

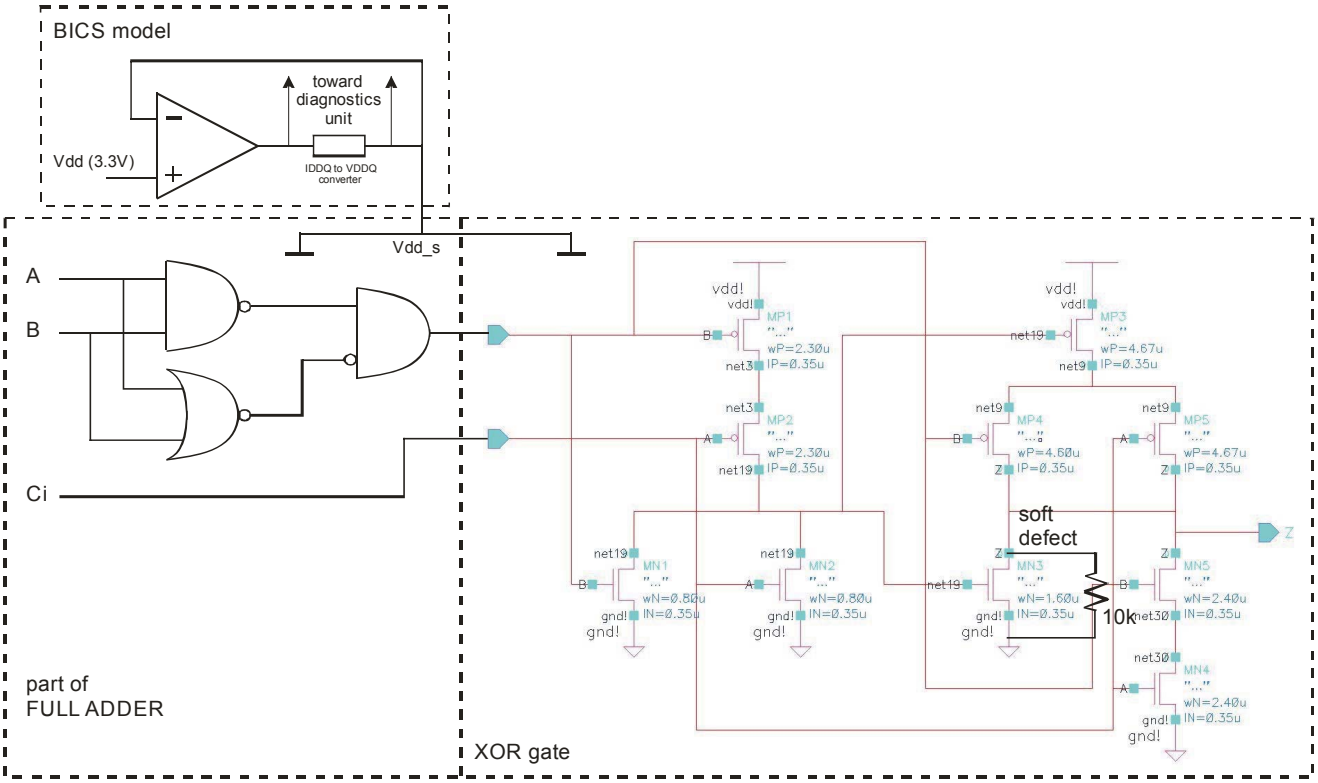


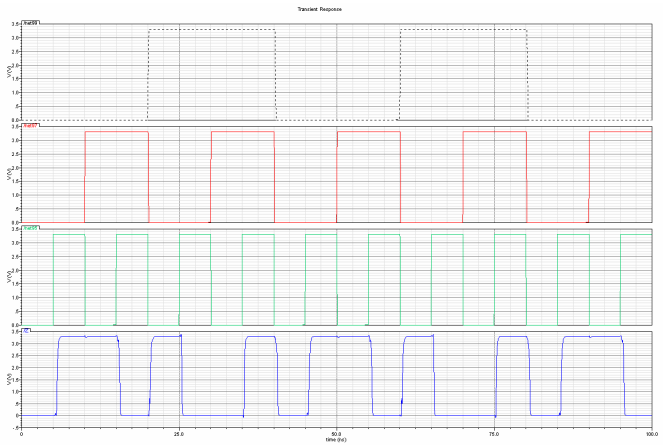
Fig. 4. Part of the Test Control Unit.

IV. Simulation Results

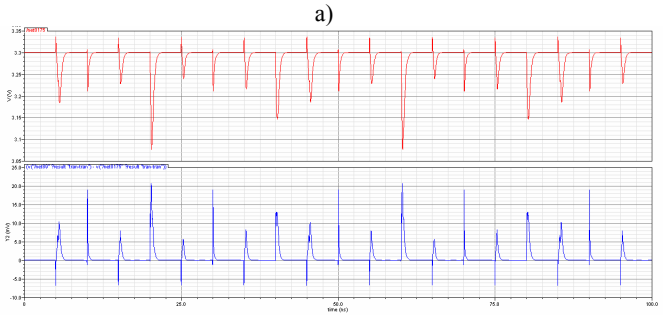
The proposed concept was verified by simulations using Cadence Virtuoso environment. Figure 4 shows the the example of full adder as the block under test. BICS is modeled with an operational amplifier and a resistor. IDDQ equivalent signal is sent to the diagnostics unit outside the IC.

This circuit was simulated twice: once as the fault free circuit, and then as the faulty circuit after one soft defect was deliberately introduced. Precisely, the leakage defect modeled as resistor connected in parallel with MN3 transistor is introduced. The block under test represents a part of the full adder that calculates the sum. It was simulated for all possible input signal combinations while observing its IDDQ. Figure 5. shows simulation results for the fault-free circuit. The waveforms of input and output signals are shown in figure 5a). Figure 5b) shows the voltage Vdd and voltage equivalent to the IDDQ (Vddq), respectively.

It can be noticed that maximal voltage noice for the power is not larger than 7.5% of its nominal value (3.3V). The signal used for diagnostics has maximal value of about 20mV that is sufficient for further processing, without any additional amplification.



a)



b)

Fig. 5. Simulation results for the fault-free circuit.

When the fault is introduced, for the same test stimuli, output voltage has almost the same waveform as the fault free circuit, as upper diagram in Figure 6. presents. Moreover, this fault will be covered with any subsequent circuit because the voltage swing covers margins for both logic states and undetectable for standard testing tools. However, IDDQ waveform (lower diagram in Figure 6) clearly shows difference with the fault free case (Figure 5.b).

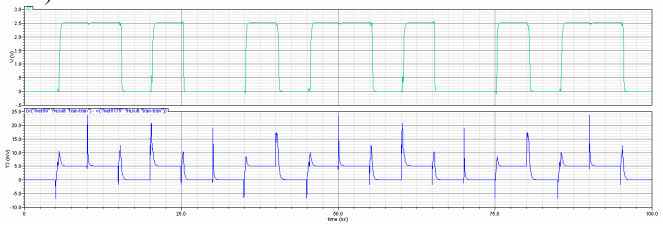


Fig. 6. Simulation results for the faulty circuit.

Due to the leakage, IDDQ voltage equivalent takes value 5mV (25% of the peak value) higher than in the fault free circuit. This amount is sufficient for diagnostic unit to distinct it from the fault free condition. Moreover, for purely testing purposes it is sufficient to check if the obtained average IDDQ matches with fault free case or not.

This undoubtedly proves that the suggested method is efficient for detecting and diagnostics even soft and other types of faults usually masked for standard Boundary scan techniques.

V. Conclusion

This paper suggests an approach for integrating IDDQ tests into SoC scan testing. The approach is based on multiplexed use of the Built-in-Current-Sensor that trades of chip area and testing efficiency. Observation of IDDQ voltage equivalent facilitates detection of soft defects. Moreover, if applied in conjunction with Boundary scan technique the method is capable to cover defects usually masked for test techniques based on logic-level monitoring. Finally, the method can be enhanced with an off-chip diagnostic unit. The approach was verified by simulations using Cadence Virtuoso environment.

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